3-dimentional analysis on the cell string current of NAND Flash memory

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In NAND Flash memory, the cell string current is very small because of large series resistances from the cells connected in series; thus, achieving the higher string current is critical for stable data sensing. Moreover, the degradation after program and erase cycles, as shown in Fig. 1, is adding the importance of the initial cell string current. Since the cell string current depends on the program states of the string, the Worst On-cell Current (WOC) is used to define the cell string current. The WOC is measured for the string with all programmed cells except the last one in the cell array.

In this paper, scaling effects on the WOC are analyzed for 70/60/50 nm NAND Flash technologies using TCAD simulation. The 3-dimentional process and device simulation methodologies have been developed and all operational features of NAND Flash (including DC, Program and Erase) except reliability concerns can be dealt with, as described in Fig. 2. We found that the 3-dimentional analysis is indispensable for the quantitative sensitivity analysis of the DC characteristics, especially for WOC. To resolve the heavy computational demands, all passing transistors (biased with V_{PASS}) are modeled as linear resistors, and its validity is verified as shown in Fig. 2(b). In order to evaluate the impacts on WOC, variety of geometrical and process parameters, such as floating-gate stack height and the ion implantation conditions, are varied and their effects are quantified. It is identified that the coupling ratio has the most significant impact on the WOC. In addition, the decrease of the WOC with the technology scaling is mostly due to the change of the coupling ratio, as shown in Fig. 3. However, the higher floating-gate stack, which is advantageous from the coupling ratio point of view, may raise the level of disturbances between the cells; thus, increasing the coupling ratio is not so easy. Possibilities of doping engineering for increasing the WOC are studied with taking the adverse effects on the program speed and leakage into accounts. The results show the importance of the surface doping in improving the WOC.

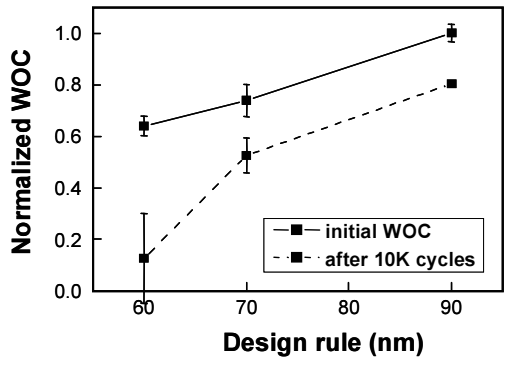

Fig. 1. Scaling trend and degradation of WOC in the NAND Flash memory.

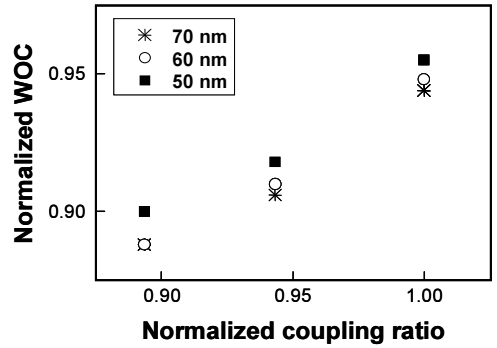

Fig. 3. The WOC in relation with the coupling ratio and the design rule.

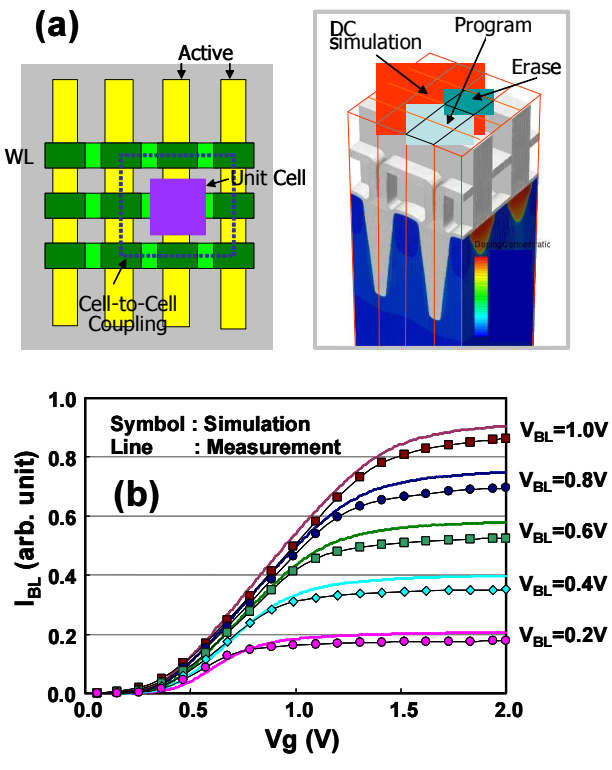

Fig. 2. (a) Schematic description of the present NAND cell simulation methodology. (b) DC simulation result to verify the accuracy of the string modeling approach.